2011

RENICE X5 CF CARD SSD Datasheet

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CATALOGUE

1. INTRODUCTION 3

1.1 PRODUCT OVERVIEW 3
1.2 FEATURE 3

2. FUNCTIONAL BLOCK DIAGRAM 4

3. PRODUCT SPECIFICATIONS 5

3.1 PHYSICAL SPECIFICATIONS 5
3.2 HOST INTERFACE 5

4. INTERFACE DESCRIPTION 6

4.1 PIN ASSIGNMENT 6
4.2 PIN DESCRIPTION 7

5. POWER SPECIFICATIONS 8

5.1 POWER SPECIFICATION 8
5.2 POWER CONSUMPTION (TYPICAL) 8

6. RELIABILITY SPECIFICATION 9

6.1 WEAR-LEVELING 9
6.2 ENDURANCE 9
6.3 H/W ECC AND EDC FOR NAND FLASH 9
6.4 MTBF 9

7. ELECTRICAL CHARACTERISTICS 10

7.1 DC CHARACTERISTICS 10
7.1.1 Definitions of VIH ,vcc,VOH,Vol 10
7.1.2 CompactFlash Interface I/O at 3.3V 10
7.1.3 Operating Conditions of Power Pins 11
7.2 INTERNAL IP CHARACTERISTICS 11
7.2.1 Power On Reset 11
7.2.2 Oscillator 11
7.2.3 2.5V Voltage Detector 11
7.2.4 2.3V Voltage Detector 12
7.2.5 Series Termination Required for Ultra DMA Operation 12
7.3 AC CHARACTERISTICS 12
7.3.1 Attribute Memory Read Timing 12
7.3.2 Configuration Register (Attribute Memory) Write Timing 13
7.3.3 Common Memory Read Timing 13

8 SOFTWARE INTERFACE 14

8.1 CF ATA COMMAND SET 14
8. 2 SMART COMMAND 15
8.2.1 SMART Data Structure (READ DATA (D0h) 16
8.3 ID TABLE INFORMATION 18
8.3.1 ID Table Information of True IDE Mode 18
8.3.2 ID Table Information of PCMCIA Mode 20

9. BUY INFORMATION 22

10. PRODUCT PART NUMBER NAMING RULE 22

1. Introduction

1.1 Product Overview

Renice X5 CF products comes with the industry standard CompactFlash form factor, provides both high performance and reliability, with great endurance working in harsh environment such as low/high temperature, great shock, vibration and interference. With these advantages and its ATA interface which is fully compatible with most popular transfer modes such as UDMA, Multiword DMA and PIO, Renice CF products is ideal storage option for embedded computing, industrial applications, network & communications, public security, military, aerospace, medical and automotive fields.

1.2 Feature

● Performance

Host Transfer rate：133MB/S

Read/Write Speed： （MB/S）

SLC：95MB/90MB

MLC：95MB/65MB

Transfer rates rating is 600x

● Form factor: 1.0 inch (42.8mmX36.4mmX3.3mm) L×W×H

● Interface standard: IDE (50Pin)

● Density：

MLC： 2GB, 4GB, 8GB, 16GB, 32GB，64GB，128GB

SLC： 2GB, 4GB, 8GB, 16GB, 32GB

● Nand flash: SLC /MLC

● Weight: 12±2g

● Input voltage: 3.3V (±5%)

● Commercial operating temperature range from 0 to +70℃

Industrial operating temperature range from -40 to +85℃

● Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm

● Supports dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology)

● ECC (Error Correction Code): Advanced 8/15 bit hardware BCH ECC engine

● Automatic sleep and wake-up mechanism to save power

● Read endurance: unlimited

● Data retention: 10 years

● MTBF: >3,000,000 Hours

2. Functional Block Diagram

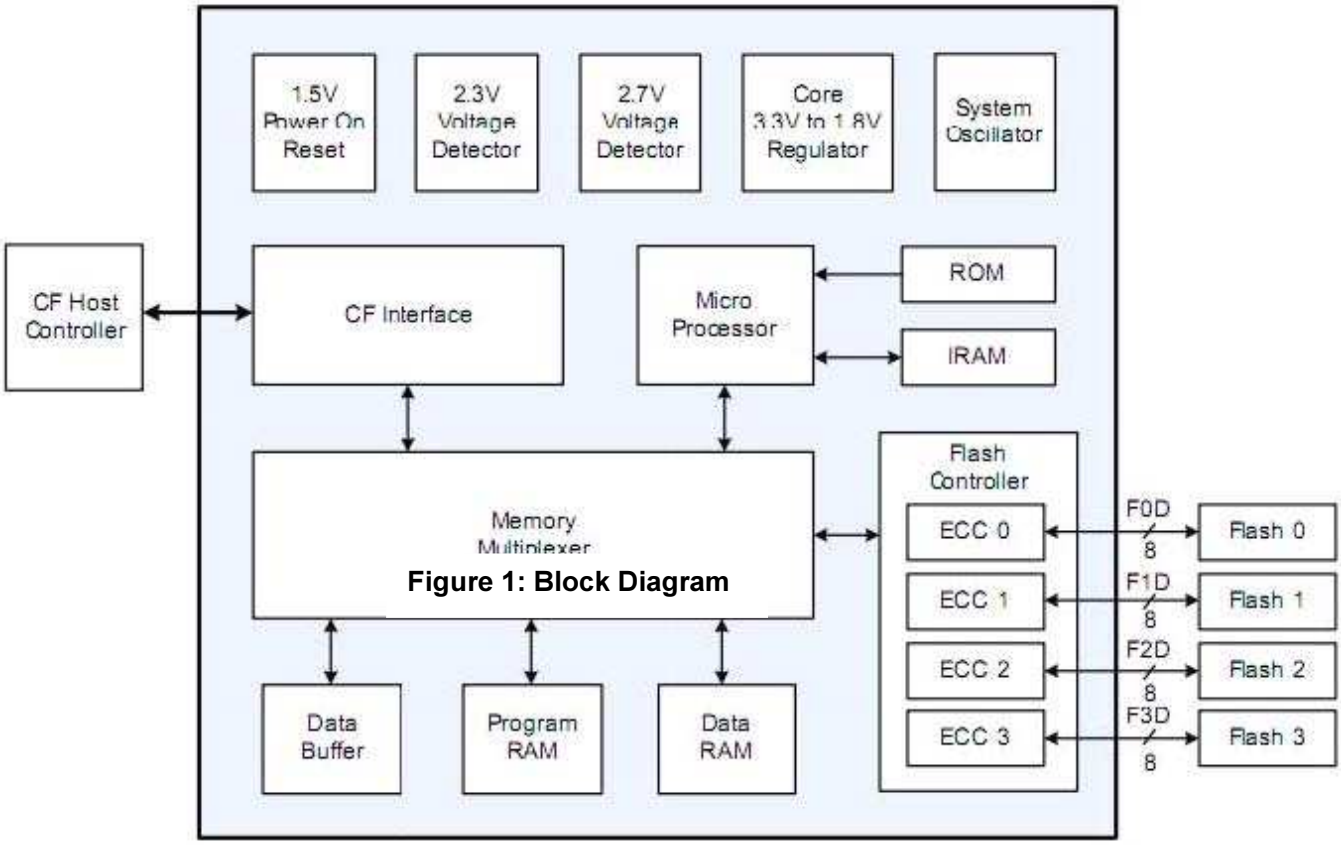
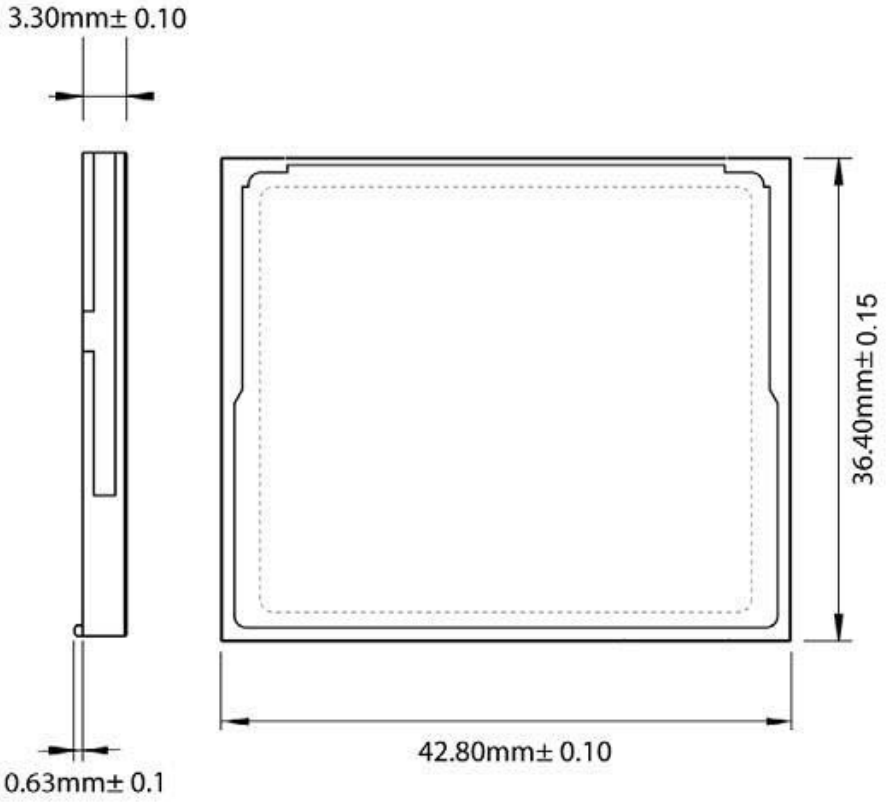


Figure 1: Block Diagram

3. Product Specifications

3.1 Physical Specifications

Form factor		1.0 inch
Dimensions(mm)	Length	42.8±0.10
	Width	36.4±0.15
	Height	3.3±0.10
Weight		12±2g
Connector		50pin IDE



3.2 Host Interface

Fully compliant with CFA 4.1 and ATA-6 Standard

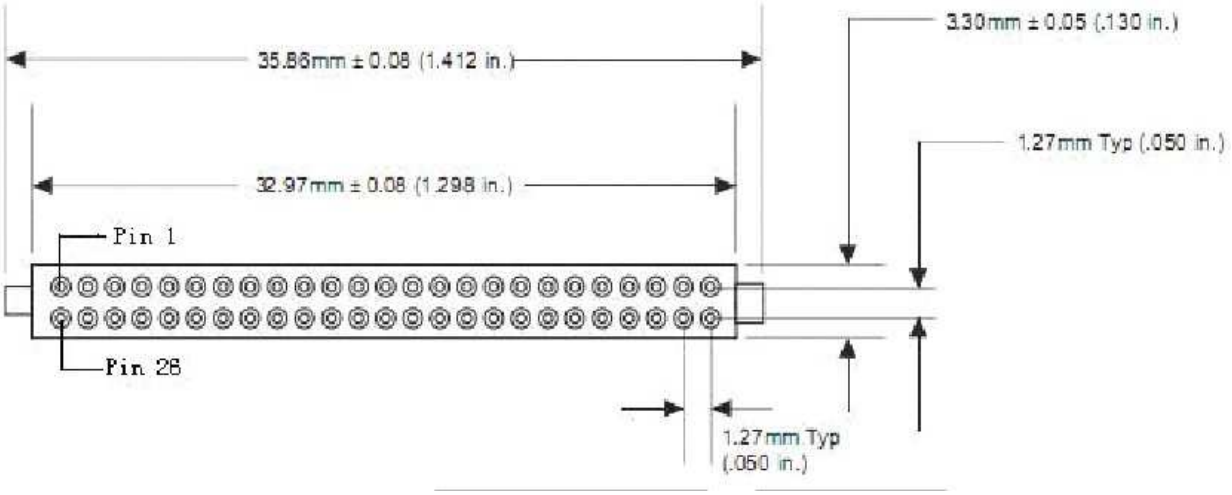
· ATA Transfer Modes:

- UDMA 0-6
- MWDMA 0-4

- PIO 0-6
- ECC (Error Correction Code) 8 or 15 bits per 512 bytes
- Supports True IDE, PC Card Memory and I/O modes

4. Interface Description

4.1 Pin Assignment



4.2 Pin Description

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I3Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
35	-IOWR STOP[10,11]	I	I3U	35	-IOWR STOP[10,11]	I	I3U	35	-IOWR[7] STOP[8,9]	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL[5]	I	I2Z	39	-CSEL[5]	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT -DDMARDY[10] DSTROBE[11]	O	OT1	42	-WAIT -DDMARDY[10] DSTROBE[11]	O	OT1	42	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1 OT1[13]
43	-INPACK -DMARQ[12]	O	OT1	43	-INPACK -DMARQ[12]	O	OT1	43	DMARQ	O	OZ1
44	-REG -DMACK[12]	I	I3U	44	-REG DMACK[12]	I	I3U	44	-DMACK[8]	I	I3U
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	I1U, ON1
46	BVD1	O	OT1	46	-STSCHG	O	OT1	46	-PDIAG	I/O	I1U, ON1
47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

5. Power Specifications

5.1 Power Specification

Operating voltage: 3.3V (±5%)

5.2 Power Consumption (typical)

Operation (Read/Write) – 0.365W

Idle – 0.018W

Sleep (Partial/Slumber) – 0.012W/0.018W

6. Reliability Specification

Item	Features	
Temperature	Operating	Standard:0~70℃
		Industrial:-40~85℃
Humidity	5-95%	
Vibration	20G(7-2000HZ)	
Shock	2,000G(@0.3ms half sine wave)	

6.1 Wear-leveling

Renice Compact Flash drive supports both static and dynamic wear-leveling, these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

6.2 Endurance

Data retention: >10 years (@25C)
Read endurance: unlimited

6.3 H/W ECC and EDC for NAND Flash

8bit/15bit ECC BCH per 512 bytes

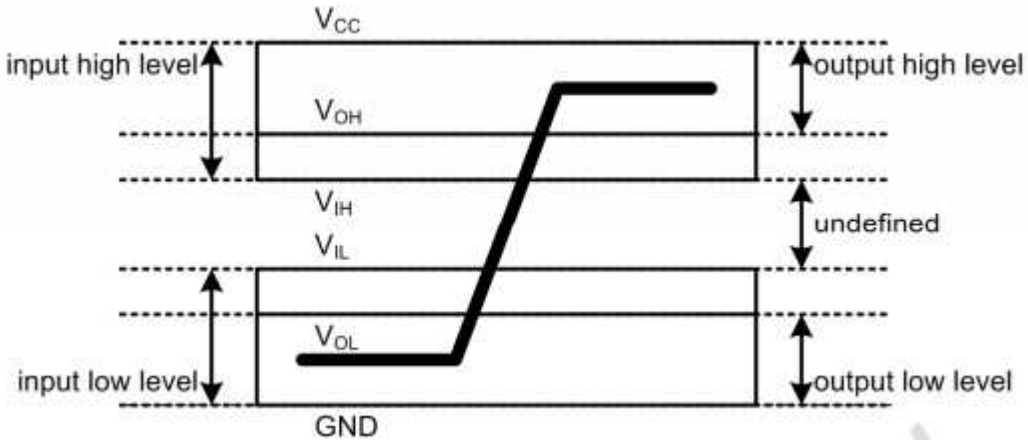
6.4 MTBF

MTBF (Mean Time between Failures) of Renice SSD: >3,000,000 hours

7. Electrical Characteristics

7.1 DC Characteristics

7.1.1 Definitions of VIH ,vcc,VOH,Vol



7.1.2 CompactFlash Interface I/O at 3.3V

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{CC}	2.97	3.63	V	
High Level Output Voltage	V_{OH}	V_{CC}-0.8		V	
Low Level Output Voltage	V_{OL}		0.8	V	
High Level Input Voltage	V_{IH}	2.4		V	Non-schmitt trigger
		2.05		V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		0.6	V	Non-schmitt trigger
			1.25	V	Schmitt trigger[1]
Pull-up Resistance	R_{PU}	52.7	141	KOhm	
Pull-down Resistance	R_{PD}	47.5	172	KOhm	

7.1.3 Operating Conditions of Power Pins

Parameter	Symbol	Min	Typ	Max	Unit
CompactFlash I/O Power	VCC3H	2.7	3.3	3.6	V
CompactFlash I/O Power at 3.3V	VCC35	3.0	3.3	3.6	V
CompactFlash I/O Power at 5V		4.5	5.0	5.5	V
Flash I/O Power	VCC3F	2.7	3.3	3.6	V
Core Power Supply	VCCK	1.62	1.8	1.98	V
Internal Oscillator Power Input	VCC18	1.62	1.8	1.98	V
Voltage Regulator Power Input	VCC3	2.97	3.3	3.63	V

7.2 Internal IP Characteristics

7.2.1 Power On Reset

Parameter	Value	Unit
Detect Voltage	1.5 (Max.)	V
Operating Voltage Range	1.6 ~ 2.0	V
Delay Time	• Rise = 3 (Max.) • Fall = 1.5 (Max.)	µs

7.2.2 Oscillator

Parameter	Value	Unit
Start-up Time	8.68 (Max.)	µs
Stand-by Current	35 (Max.)	µA
Frequency Stability	30 ~ 80	MHz

7.2.3 2.5V Voltage Detector

Parameter	Value	Unit
Detect Voltage	2.5 (Max.)	V
Operating Voltage Range	1.6 ~ 3.6	V
Delay Time	• Rise = 3 (Max.) • Fall = 1.5 (Max.)	µs

7.2.4 2.3V Voltage Detector

Parameter	Value	Unit
Detect Voltage	2.3 (Max.)	V
Operating Voltage Range	1.6 ~ 3.6	V
Delay Time	• Rise = 3 (Max.) • Fall = 1.5 (Max.)	µs

7.2.5 Series Termination Required for Ultra DMA Operation

The CF provides embedded termination resistors for operation in any of the Ultra DMA modes.The following table describes typical values for series termination at the device.

CF Signal	Device Termination
HIOE#	82 ohm
HIOW#	82 ohm
CE1#, CE2#	82 ohm
HA[2:0]	82 ohm
HREG#	82 ohm
HD[15:0]	33 ohm
DMARQ	22 ohm
HIRQ	22 ohm
IORDY	22 ohm
HRST	82 ohm

7.3 AC Characteristics

7.3.1 Attribute Memory Read Timing

Speed Version		300		
Item	Symbol	Min	Max	Unit
Read Cycle Time	tc(R)	300		ns
Address Access Time	ta(HA)		300	ns
Card Enable Access Time	ta(CEx)		300	ns
Output Enable Access Time	ta(HOE)		150	ns

Output Disable Time from CEx#	tdis(CEx)		100	ns
Output Disable Time from HOE#	tdis(HOE)		100	ns
Address Setup Time	tsu(HA)	30		ns
Output Enable Time from CEx#	ten(CEx)	5		ns
Output Enable Time from HOE#	ten(HOE)	5		ns
Data Valid from Address Change	tv(HA)	0		ns

NOTE: All times intervals are recorded in nanoseconds. HD refers to data provided by the Compact Flash Card to the system. The CEx# signal or both the HOE# signal and the HWE# signal are deasserted between consecutive cycle operations

7.3.2 Configuration Register (Attribute Memory) Write Timing

Speed Version		250 ns		Unit
Item	Symbol	Min	Max	
Write Cycle Time	tc(W)	250		ns
Write Pulse Width	tw(HWE)	150		ns
Address Setup Time	tsu(HA)	30		ns
Write Recovery Time	trec(HWE)	30		ns
Data Setup Time for HWE#	tsu(HD-HWEH)	80		ns
Data Hold Time	th(HD)	30		ns

NOTE: All times intervals are recorded in nanoseconds. HD refers to data provided by the system to the Compact Flash Card.

7.3.3 Common Memory Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns		Unit
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Output Enable Access Time	ta(HOE)		125		60		50		45	ns
Output Disable Time from HOE#	tdis(HOE)		100		60		50		45	ns
Address Setup Time	tsu(HA)	30		15		10		10		ns
Address Hold Time	th(HA)	20		15		15		10		ns
CEx# Setup before HOE#	tsu(CEx)	5		5		5		5		ns
CEx# Hold following HOE#	th(CEx)	20		15		15		10		ns
Wait Delay Falling from HOE#	tv(IORDY-HOE)		35		35		35		na[1]	ns
Data Setup for Wait Release	tv(IORDY)		0		0		0		na[1]	ns
Wait Width Time[2]	tw(IORDY)		350		350		350		na[1]	ns

8 Software Interface

8.1 CF ATA Command Set

The CF supports the CF-ATA command set shown as below.

Command	C	Protocol
General Feature Set		
Execute Drive Diagnostic	9	Device diagnostic
FlushCache	E	Non-data
Identify Device	E	PIO data-in
Read DMA	C	DMA
Read Multiple	C	PIO data-in
Read Sector(s)	2	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	E	Non-data
Set Multiple Mode	C	Non-data
WriteDMA	C	DMA
Write Multiple	C	PIO data-out
Write Sector(s)	3	PIO data-out
NOP	0	Non-data
Read Buffer	E	PIO data-in
Write Buffer	E	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
SecurityMode Feature Set		
Security SetPassword	F	PIO data-out
Security Unlock	F	PIO data-out
Security Erase Prepare	F	Non-data
Security Erase Unit	F	PIO data-out
Security Freeze Lock	F	Non-data
Security Disable Password	F	PIO data-out
SMART Feature Set		
SMART Disable Operations	B	Non-data
SMART Enable/Disable Autosave	B	Non-data

SMART Enable Operations	B	Non-data
Command	Code	Protocol
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-in
Host Protected Area Feature Set		
Read NativeMax Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max SetPassword	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
CFA FeatureSet		
CFA RequestExtended Error Code	03h	Non-data
CFA Write Sectors Without Erase	38h	PIO data-out
CFA Erase Sectors	C0h	Non-data
CFA Writer Multiple Without Erase	CDh	PIO data-out
CFA Translate Sector	87h	PIO data-in
Set FeaturesEnable/Disable 8-bit	EFh	Non-data
Others		
Format Track	50h	PIO data-out
Initialize Drive Parameters	91h	Non-data
Recalibrate	1Xh	Non-data
Seek	7Xh	Non-data
Wear Level	F5h	Non-data
Write Verify	3Ch	PIO data-out

8. 2 SMART Command

The CF supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit. Users can obtain the data using the “Read Data” command.

Valu	Command	Valu	Command
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

SMART Feature Register Values

If there served size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh).

8.2.1 SMART Data Structure (READ DATA (D0h)

Byte	F / V	Description
0 - 1	X	Revision code
2 - 114	X	Vendor specific
115 - 116	V	Power cycle count of the device
117 - 361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware Version/Date Code
396 - 397	F	Number of initial invalid block (396 = MSB, 397 = LSB)

Byte	F / V	Description
398 - 399	V	Number of run time bad block (398 = MSB, 399 = LSB)
400	V	Number of spare block
401-402	V	Erase count
403-405	F	'SMI'
406	F	Number of max pair
407-510	X	Vendor specific
511	V	Data structure checksum

NOTE:

F = content (byte) is fixed and does not change.

V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

X = content (byte) is vendor specific and may be fixed or variable.

R = content (byte) is reserved and shall be zero.

N = Nth Management Unit

*4 Byte value: [MSB] [2] [1] [LSB]

8.3 ID Table Information

8.3.1 ID Table Information of True IDE Mode

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the Compact Flash Storage Card
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order inWord
27-46	XXXXh	40	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58= MSW)
59	0100h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h.
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multi word DMA transfer cycle time per word. In PCMCIA mode this value shall be0h.
66	0078h	2	Recommended Multi word DMA transfer cycle time. In PCMCIA mode this value shall be 0h.

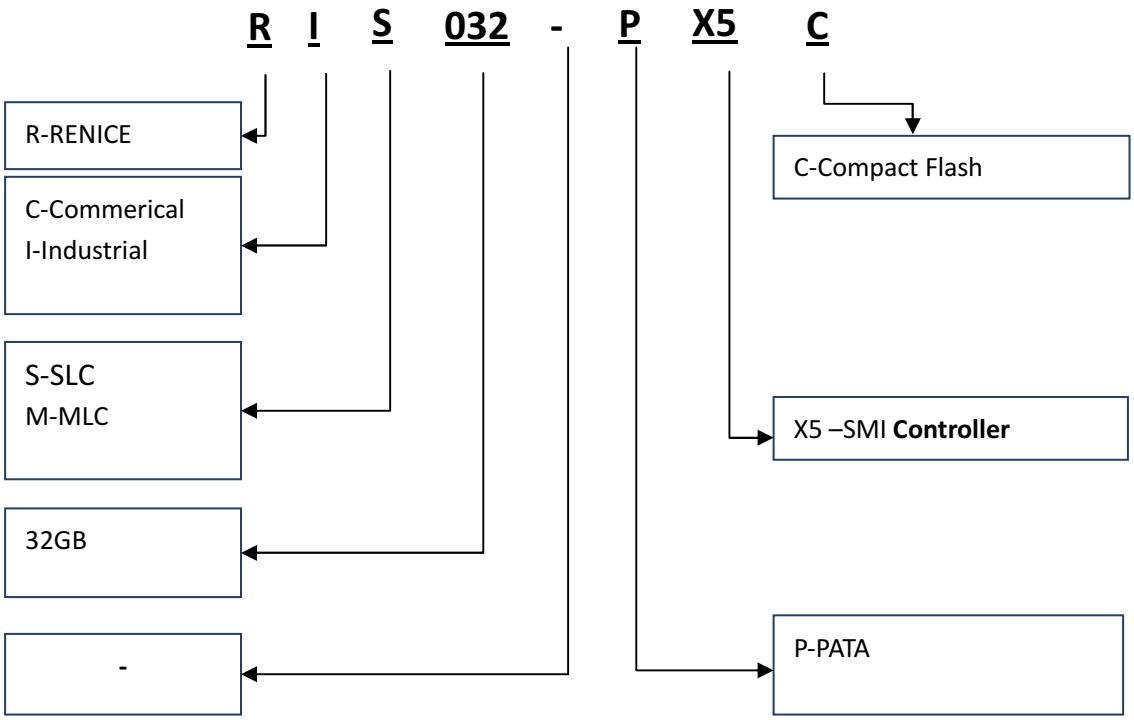
Word Address	Default Value	Total Bytes	Data Field Type Information
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80	0000h	2	Major version number
81	0000h	2	Minor version number
82	7028h	2	Command sets supported
83	500Ch	2	Command sets supported
84	4000h	2	Command sets supported
85	0000h	2	Command sets Enable
86	0000h	2	Command sets Enable
87	0000h	2	Command sets Enable
88	007Fh	2	Ultra DMA mode supported and selected Default: Ultra DMA mode 6
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	0000h	2	Master Password Revision Code
93	604Fh 6F00h 603Fh	2	• Hardware reset result (Master) • Hardware reset result (Slave) • Hardware reset result (Master w/ slave present)
94-127	0000h	68	Reserved
128	0000h	2	Security status
129-159	0000h	64	Vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0092h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	• CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting • 80ns cycle in memory and I/O mode
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

8.3.2 ID Table Information of PCMCIA Mode

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order inWord
27-46	XXXXh	40	Model number in ASCII (Left justified). Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0200h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0003h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58= MSW)
59	0100h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable inLBA Mode
62	0000h	2	Reserved
63	0000h	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h.
64	0003h	2	Advanced PIO modes supported
65	0000h	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h.
66	0000h	2	Recommended MultiwordDMA transfer cycle time. In PCMCIA mode this value shall be 0h.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control

69-79	0000h	20	Reserved
80	0000h	2	Major version number
81	0000h	2	Minor version number
82	7028h	2	Commandsets supported 0
83	500Ch	2	Commandsets supported 1
84	4000h	2	Commandsets supported 2
85	0000h	2	Commandsets Enable 0
86	0000h	2	Commandsets Enable 1
87	0000h	2	Commandsets Enable 2
88	0000h	2	Ultra DMA supported and selected
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	0000h	2	Reserved
93-127	0000h	70	Reserved
128	0000h	2	Security status
129-159	0000h	64	Vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	8D9Bh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability Default: UltraDMA mode 6
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

9. Buy Information

Capacity	MLC Part Numbers	SLC Part Numbers
2GB	RCM002-PX5C	RCS002- PX5C
4GB	RCM004-PX5C	RCS004- PX5C
8GB	RCM008-PX5C	RCS008- PX5C
16GB	RCM016-PX5C	RCS016- PX5C
32GB	RCM032-PX5C	RCS032- PX5C
64GB	RCM064-PX5C	N
128GB	RCM128-PX5C	N

10. Product Part Number Naming Rule